HARDWARE
USER MANUAL

MODEL 2165

PUBLICATION NO. 980898-001

RACAL INSTRUMENTS

United States

(Corporate Headquarters and Service Center)
4 Goodyear Street, Irvine, CA 92618
Tel: (800) 722-2528, (949) 859-8999; Fax: (949) 859-7139

5730 Northwest Parkway Suite 700, San Antonio, TX 78249
Tel: (210) 699-6799; Fax: (210) 699-8857

Europe

(European Headquarters and Service Center)
18 Avenue Dutartre, 78150 LeChesnay, France
Tel: +33 (0)1 39 23 22 22; Fax: +33 (0)1 39 23 22 25

29-31 Cobham Road, Wimborne, Dorset BH21 7PF, United Kingdom
Tel: +44 (0) 1202 872800; Fax: +44 (0) 1202 870810

Via Milazzo 25, 20092 Cinisello B, Milan, Italy
Tel: +39 (0)2 6123 901; Fax: +39 (0)2 6129 3606

Racal Instruments Group Limited, Technologie Park, D-51429 Bergisch Gladbach, Germany
Tel: +49 2204 844205; Fax: +49 2204 844219

info@racalinstruments.com
sales@racalinstruments.com
helpdesk@racalinstruments.com
http://www.racalinstruments.com
info@racalinstruments.de
www.racalinstruments.de

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E-Mail:	Helpdesk@racalinstruments.com	
Telephone:	+1 800 722 3262	(USA)
	+44(0) 8706 080134	(UK)
Fax:	+1 949 859 7309	(USA)
	+44(0) 1628 662017	(UK)

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Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.
2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

Racal Instruments

EC Declaration of Conformity

We

Racal Instruments Inc.
4 Goodyear Street
Irvine, CA 92618

declare under sole responsibility that the

2165 PXI Digitizer, P/N 407946

conforms to the following Product Specifications:

EMC: EN61326:1997 + A1:1998 + A2:2001, Class A

Safety: EN61010-1:1993 + A2:1995

Supplementary Information:

The above specifications are met when the product is installed in a Racal Instruments certified mainframe with faceplates installed over all unused slots, as applicable

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (modified by 93/68/EEC).

Irvine, CA, January 3, 2005: Director of Engineering

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Introduction

The Racal Instruments' Model 2165 is a dual-channel PXI-based high speed Waveform Digitizer card in a compact 3U PXI module. The two channels are completely separate and each channel has it's own 14 bit, 70 MSPS Analog to digital converter. This structure ensures low crosstalk and no phase error between the channels. Figure 1 shows the functional block diagram for the 2165.

On the left side of the diagram are the differential analog inputs, the external clock in- /output and the external trigger input. The analog input is a differential input. By switching one input to ground or to the programmable DC Offset source it becomes a single ended input with programmable DC mid level. The input has six range steps. If desired the analog signal can be filtered to remove out of band noise. The EXTERNAL CLOCK is the sample clock in- or output. The two channels can sample simultaneously or at different, independent speeds. The TRIGGER input allows the user to control the start of data capture with external triggering.

After the 14 bit analog to digital conversion there is the 512k RAM capture memory
When the 2165 is triggered, capture memory starts running from its start address.
During the measurement an internal or external clock increments the memory counter. When the counter reaches the value of the stop address it jumps back to the start address, or stops if the loop mode is programmed off.

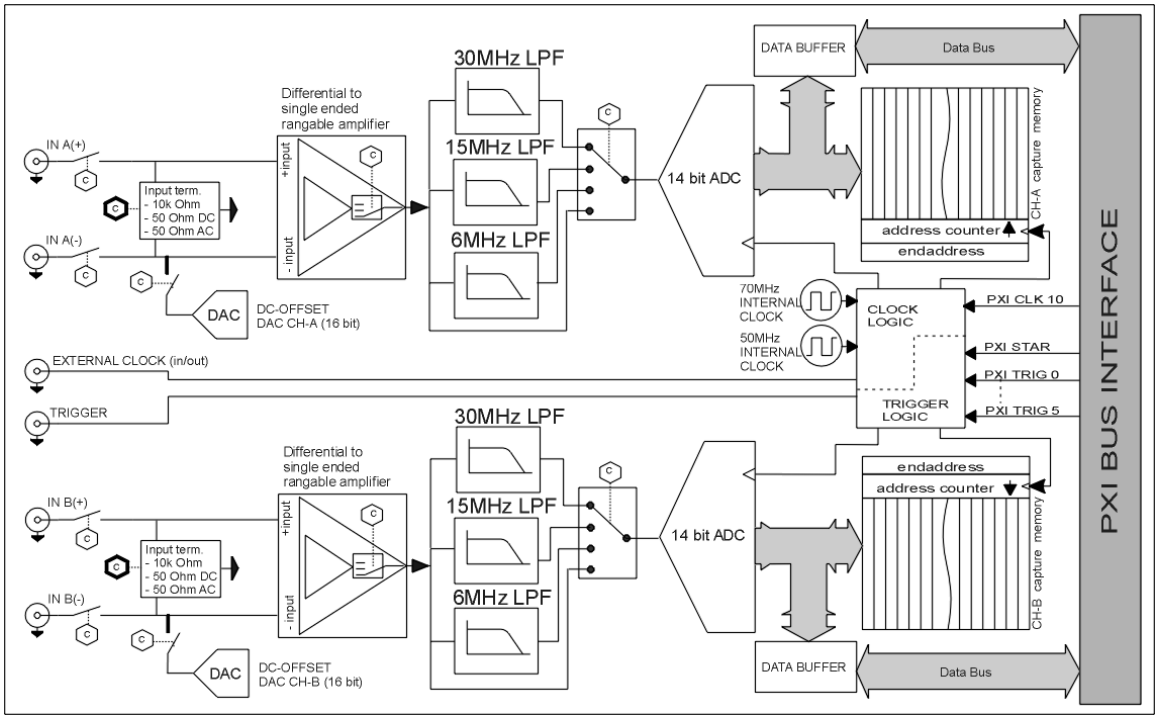

Figure 1 2165 Functional Block Diagram

1 Analog Circuit

The SMB connectors labeled A+, A- ,B+ and B-, on the front of the 2165, are the analog differential inputs for Channel A and Channel B. If a channel is set in the single input mode the input signal must be connected to the + input. The negative input is connected to ground by the software.

1.1 Input Coupling

Figure 2 shows the analog input circuit from one input. The analog input impedance is selectable, 50Ω AC, 50Ω DC or 10kΩ DC. If the analog input is disconnected, the internal circuit is disconnected from the input by a mechanical switch. The settings for the input mode are separate for each channel, so Channel A can be 50Ω AC differential input, while channel B is 10kΩ DC single input.

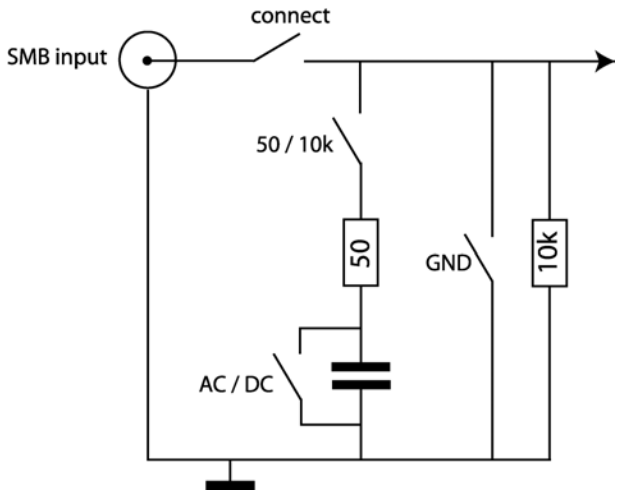

Figure 2 Analog Input Circuit

1.2 Input Ranges:

The 2165 offers six ranges to optimize the ADC resolution to the input signal.

Input Range	Input DC offset
1Vpp	+5V…-5V
2Vpp	+5V…-5V
4Vpp	+5V…-5V
5Vpp	+25V…-25V
10Vpp	+25V…-25V
20Vpp	+25V…-25V

Table 1 Input Ranges 2165

1.3 Input Offset

At the input of the 2165 there is a 16 bit offset DAC. The input offset positions an input signal around a DC value. Depending on the range, the input offset span is +5Volt to –5Volt or +25Volt to – 25Volt (Table 1). When the input offset is used the negative connector from the differential input is disabled.

Example: Examine a signal (1Vtt) on a 1 Volt DC offset, see Figure 3. The top of the input signal is 1Volt offset + 0.5V signal = 1.5Vpeak input voltage. Without using input offset, you would need to specify a range of 4Vtt to capture the waveform. In this case a large range from the ADC will not be used because of the DC voltage on the signal. However, with the input offset set to 1Volt, the signal centers around 0V and a range of 1Vtt is enough to capture the signal. This improves the accuracy of the measurement.

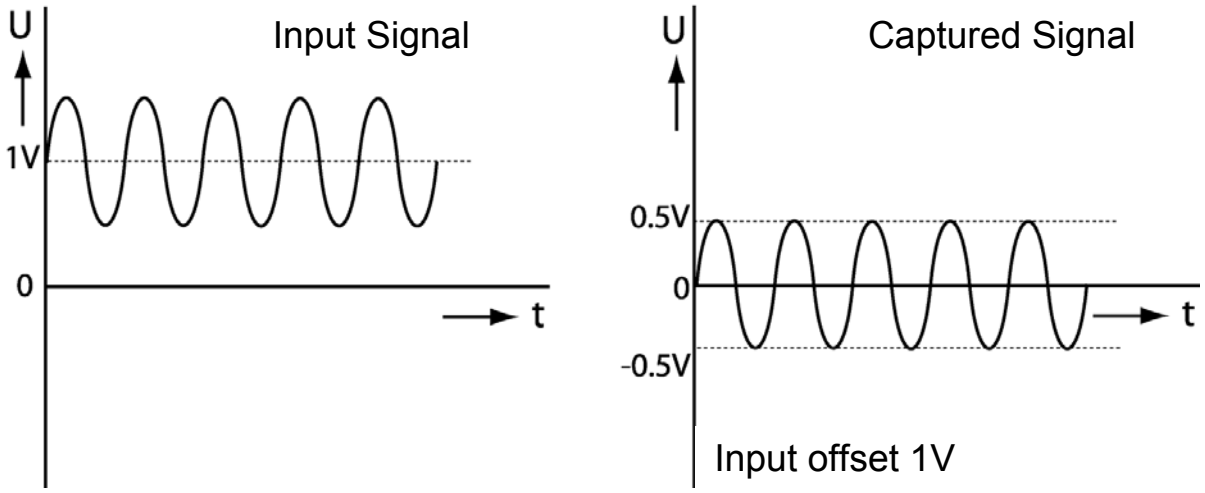

Figure 3 Input Offset

1.4 Filters

Each channel has three selectable 3-pole low pass filters. The filters limit the bandwidth of the signal path and is useful for rejecting out of band noise. The selectable filters have cutoff frequencies of: 6 MHz, 15 MHz, and 30 MHz. The filters can also be bypassed for wideband signals. Figure 4 has the typical frequency response of the 2165.

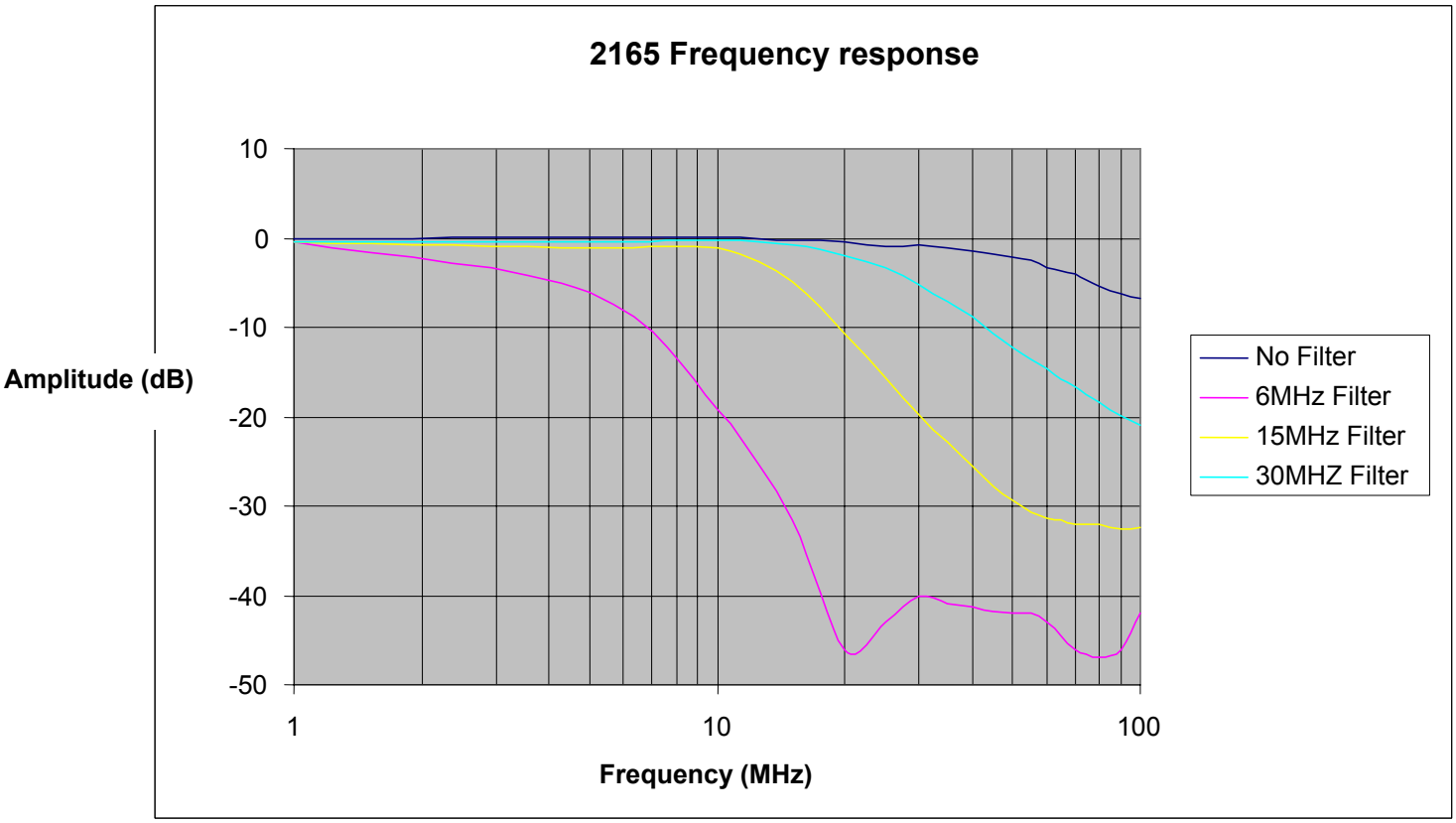

Figure 4 Typical Frequency Response

2 Triggering

The 2165 starts data capture on a triggered signal. The separate trigger circuits from Channel-A and Channel-B allow each channel to start on different trigger sources and on different trigger edges or levels. The 2165 can trigger on three trigger sources: Digital input trigger, Software trigger and Analog trigger. Figure 5 shows the trigger capabilities. To prevent triggering during connection or initializing there is a lock bit. The 2165 can be triggered once the lock bit is set.

2.1 Digital Input Triggering

The digital trigger accepts triggers from the front panel trigger and the PXI back plane trigger sources including PXI TRIGGER 0 to 5 and PXI STAR TRIGGER. The front panel trigger input uses normal TTL logic levels, with a 0.5V nominal threshold for a low level and a 2V nominal threshold for a high level.
All the trigger inputs except the software trigger can handle different trigger signals. It is possible to trigger on positive and negative level or positive and negative edge trigger signals.
For settings see the “SET TRIGGER” command in the DLL functions.
In level trigger mode the capturing starts when trigger goes active and stops when trigger goes inactive. Edge trigger mode has two options, normal or continuous. In normal mode the data capture starts at a trigger edge and stops on the next trigger edge. In continuous mode the measurement runs until stopped by the software. Every measurement can be stopped with the software by forcing the channel out of “lock mode”. When the module is out of lock mode the trigger register will be cleared.

2.2 Software Triggering

If trigger timing is not a issue, there is a software initiated trigger. By writing the trigger register the data capture can be started or stopped.

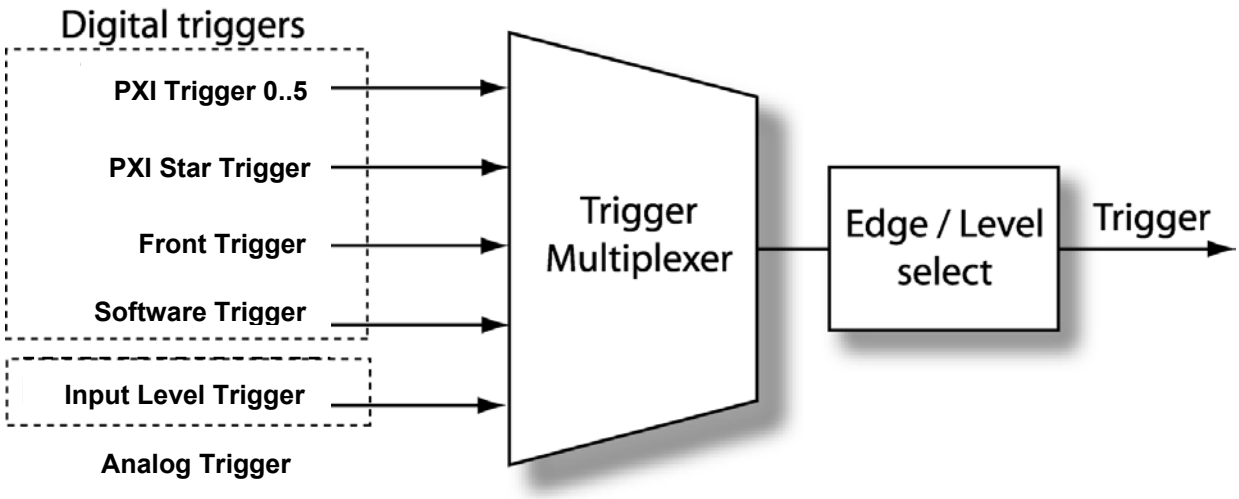

Figure 5 2165 Trigger Capabilities

2.3 Analog Triggering

In the analog trigger mode the analog input signal starts and stops the data capture. The trigger signal is extracted from the zero crossing from the input signal. (ADC code 4000 Hex).
If the analog input voltage is higher than 0 volt the trigger signal is high and if the analog input voltage is lower than 0 the trigger signal is low. Trigger at another analog level by adding an input offset voltage with the input offset DAC. With the level and edge trigger settings it is possible to capture different parts from the analog input signal. In the positive or negative level trigger mode data capture starts when the analog input signal is higher or lower than 0 volt. In this mode only the upper parts or the lower parts from the analog signal will be captured. (Figure 6) In edge trigger mode data capture starts at a trigger edge and stops on the next trigger edge. This edge can be negative or positive according to the setting. (Figure 7)
In continuously trigger mode the capturing starts on a positive or negative edge and runs till the memory stop address is reached (not loop mode) or stopped by the user in loop mode. (Figure 8)

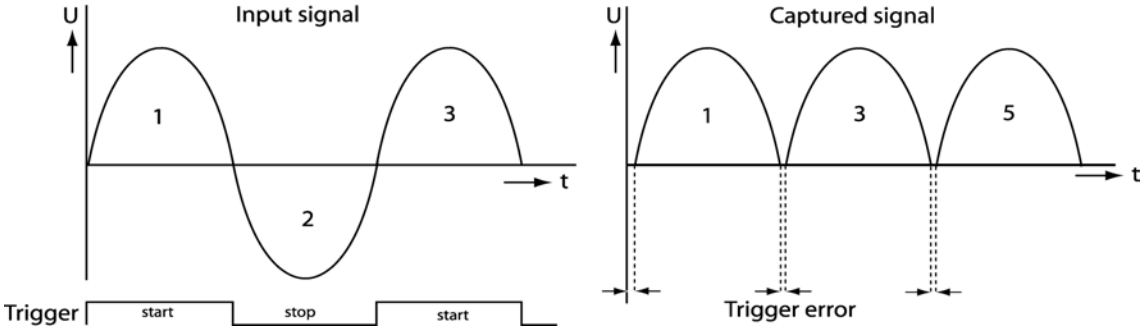

Figure 6 Analog Positive Level Triggering

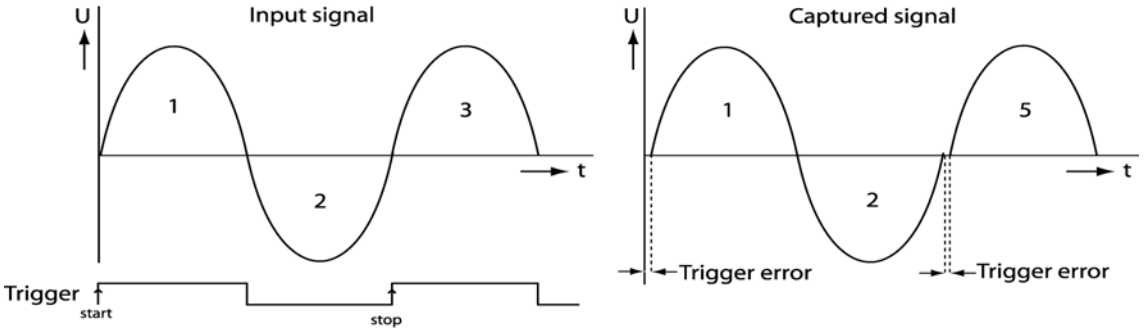

Figure 7 Analog Positive Edge Triggering

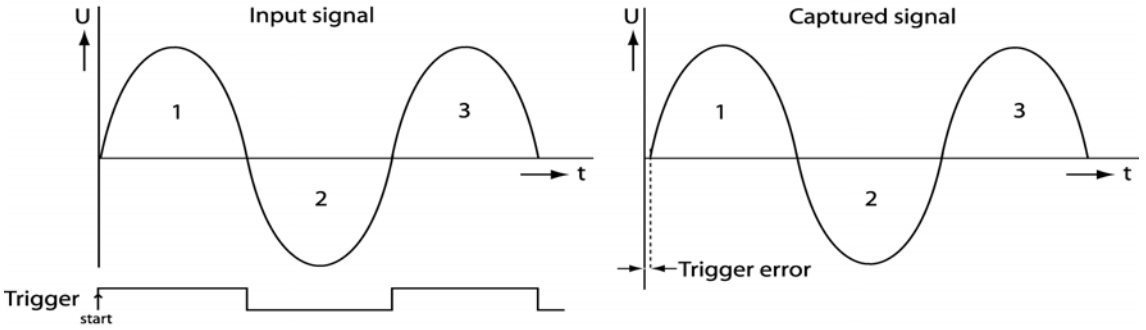

Figure 8 Analog Positive Continuous Edge Trigger

2.4 Trigger Timing

The external trigger can come from the front panel trigger input or the PXI back plane trigger sources. The external trigger input uses normal TTL logic levels, with a 0.5V nominal threshold for a low level and a 2V nominal threshold for a high level. The trigger signal is related to the sample clock, and needs one sample clock cycle to clock into the trigger register. The trigger must be high 6ns before the rising edge from the sample clock to start or stop the measurement (see Figure 9 and Figure 10). The ADC has a latency of 8 sample clock pulses, the first sample that will be saved after triggering is the sample taken 8 sample clocks before triggering. When the measurement is stopped with the trigger signal or by reaching the stop-address the last sample that will be saved is a sample taken eight sample clocks before the stop condition (see Figure 9 and Figure 10).

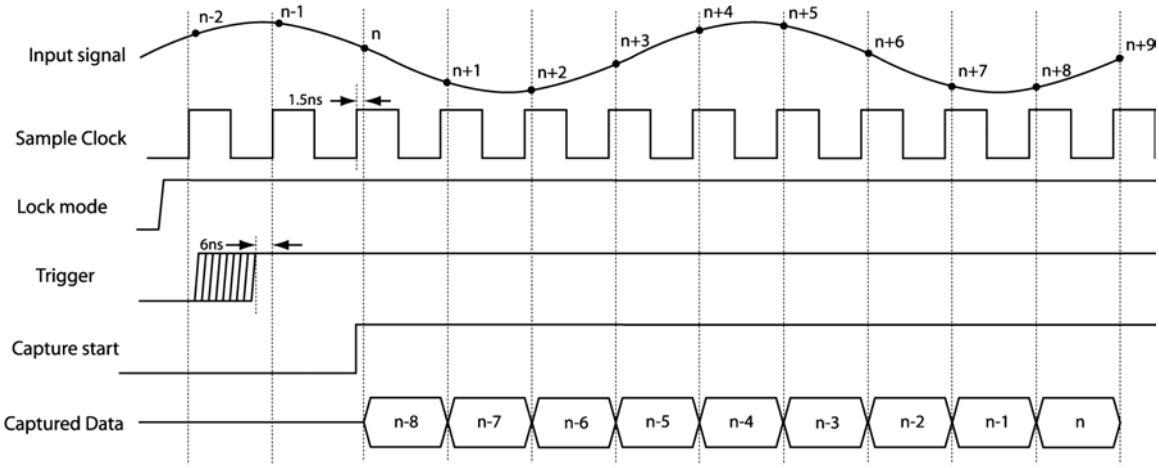

Figure 9 External trigger timing start

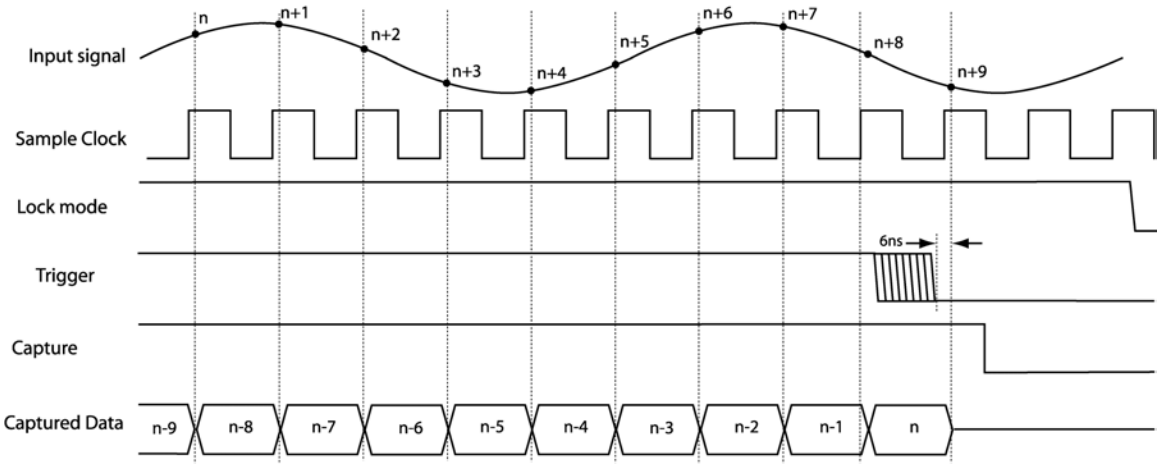

Figure 10 External trigger timing stop

3 Clocking

The 2165 can sample on different clock signals. The module has two internal clock sources, 70MHz and 50MHz and an external clock source input. To sample lower clock frequencies it is possible to divide the clock source to a lower frequency with the onboard divider. The divider can divide by a maximum of 256. Both channels have their own clock-divider, so they can capture data using different frequencies.
If an application requires sampling at specific intervals that cannot be achieved by using the internal 70MHz or 50 MHz clock, an external sample clock can be used. The external clock can be input via the SMB connector. When the front clock connector output is enabled, the sample clock from channel-A is present on this connector. This clock can be used to synchronize other devices in a measurement system via the 2165. The front panel clock in and- output has a 50-Ohm termination.

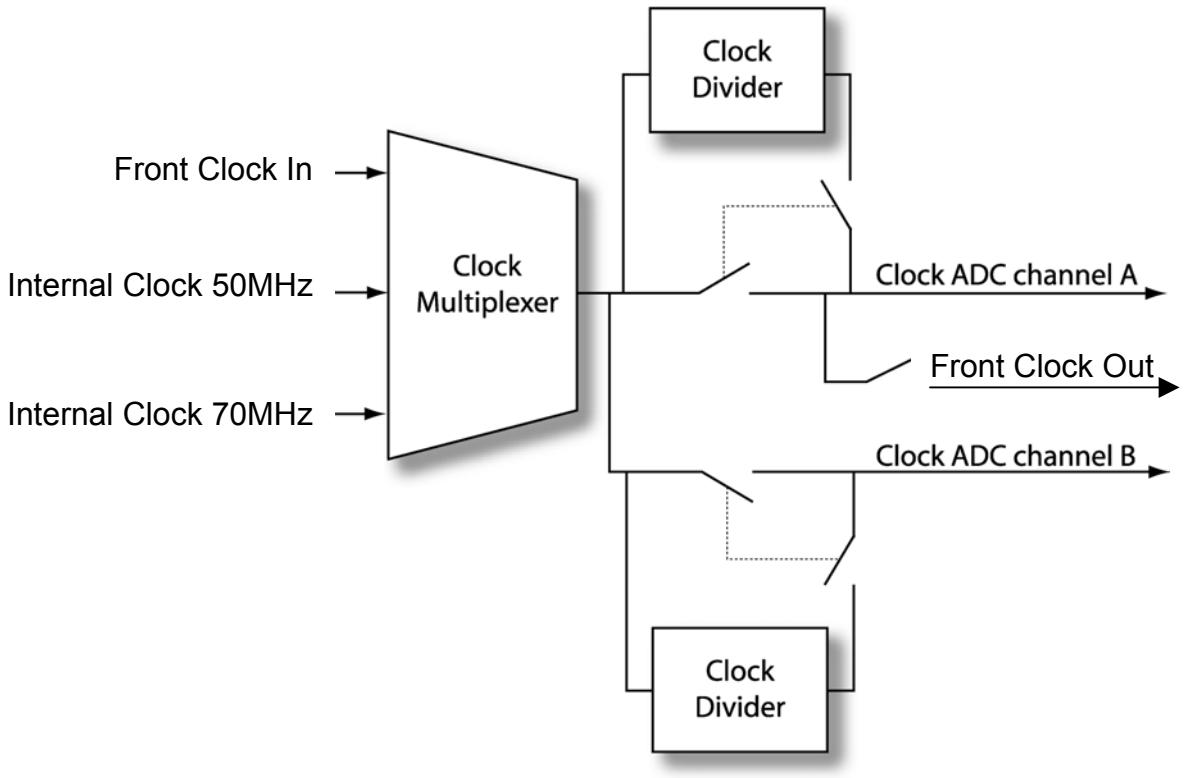

Figure 11 Clock circuit

4 Onboard Memory

The onboard memory is for captured data storage before transfer to the computer. This capture memory has 512k words available for each channel. The capture memory of the 2165 is addressed through a counter. This counter is active during data capture and during reading or writing the memory via the bus. In capture mode the counter starts counting from the start and increments on each sample clock until it reaches the end address from the memory (7FFFF Hex). At the end of the memory the counter stops, or jumps to address 00000 Hex and counts up again. This selection is set with the loop mode-bit in the 2165 register, see (Figure 12). In this register there is also a address to see if the channel has reached the end address, the loop status register. See the **Register Assignment** for details. The start address should be written to the appropriate registers before the pattern starts. When writing the start address, this value is also loaded into the counter. In bus access mode the same mechanism is active except that the clock is now the read or write signal. To write a memory section the start address should be set first. The counter is now pointing to the start address and the content of this address can be read or written. After each read or write the counter increments to the next address allowing burst read or write actions. Note that the counter will stop or jump back to the start address when it reaches the end address, depending of the loop mode-bit in the PD register.
Since the memory may not be read or written during pattern generation, there is a lock bit that should be set to allow pattern generation. The memory is then locked for reading or writing. After setting the lock bit to unlock the memory is accessible again. A measurement that was running at that moment will be aborted.

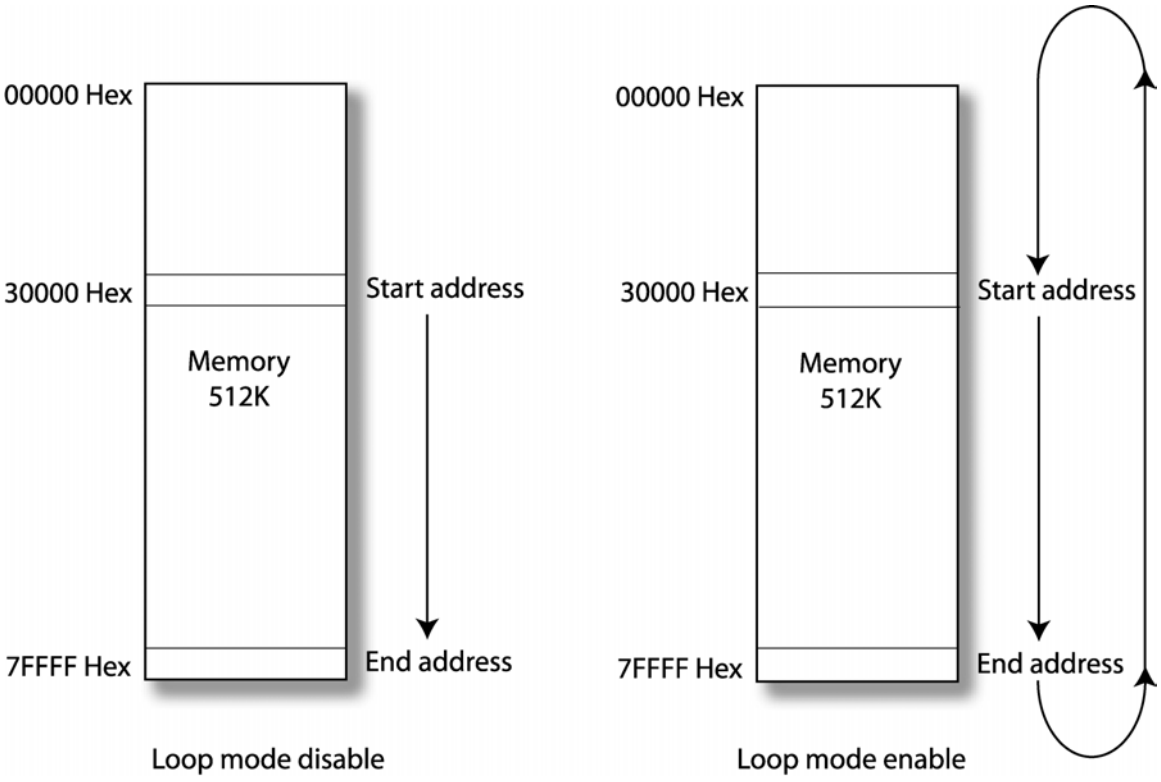

Figure 12 Function of the loopmode-bit

5 Calibration

Calibration is a test that compares the values indicated by the 2165 with an external reference source. The result of a calibration is used to determine the gain and offset error so the 2165 can correct the error with the trim DAC's.
For optimum performance use self-calibration when the digitizer is placed in a new system or if the temperature changes more than 5°C from the previous calibration
The maximum recommended amount of time between two calibrations is six months.

The calibration can be done with the software tool **2165 calibration** (980898-004) or with the DLL function **2165_AutoCalibrate**.
The input offset DAC is used as reference voltage source. Before the auto calibration is started the input offset DAC must be calibrated first, using a calibrated high-precision voltmeter connected to the negative input.
The 2165 uses trim DAC's to calibrate the offset and gain errors of the analog input channels. Once the calibration process is done, the calibration constant will be stored in EEPROM. These values can be loaded by the software, and used as needed by the board.
The software tool leads you step for step through the calibration process, and for details of the DLL function see the **2165 Software Manual** (980898-002).

6 Register assignment:

Channel A

ADDRESS	Operation	DATA	Description
01 Hex	R and W	00000 : 3FFFF Hex	Read or write address counter
02 Hex	R and W	0000 : FFFF (auto increment)	Read or write to memory
04 Hex	W	00 : FF Hex	Write clock source divider (ADC)
05 Hex	R	00 Hex No channel has looped 01 Hex Channel A has looped 02 Hex Channel B has looped 03 Hex Channel A and B looped	Read loop status. Displays if the memory counter has looped one time.
06 Hex	R and W	00 Hex No trigger 01 Hex Trigger channel A 02 Hex Trigger channel B 03 Hex Trigger channel A and B	Write software trigger start. Read current trigger status
07 Hex	W	00 Hex Front clock input 01 Hex Internal clock 70MHz 02 Hex Internal clock 50MHz 10 Hex Front clock out enable	Select Clock source. and Clock output function.
08 Hex	R and W	01 Hex No filter 02 Hex 6MHz filter 04 Hex 15MHz filter 08 Hex 30MHz filter	Select Filter (Combine with Analog output select code)
08 Hex	R and W	10 Hex range 1 input = 1Vpp (x0.2 = 5Vpp) 20 Hex range 2 input = 2Vpp (x0.2 = 10Vpp) 40 Hex range 3 input = 4Vpp (x0.2 = 20Vpp)	Select Attenuator (Combine code with Filter select and input offset)
08 Hex	R and W	80 Hex Input offset on	Input offset on / off (combine with ATT)
09 Hex	R and W	01 Hex Connect input A+ 02 Hex Connect input A- 04 Hex Input A+ 50 Ohm 08 Hex Input A- 50 Ohm 10 Hex Input A+ to GND 20 Hex Input A- to GND 40 Hex input attenuation x 0.2 80 Hex Both inputs AC coupling	Analog output select
0A Hex	W	00 Hex Front trigger 01 Hex PXI trigger 0 02 Hex PXI trigger 1 03 Hex PXI trigger 2 04 Hex PXI trigger 3 05 Hex PXI trigger 4 06 Hex PXI trigger 5 07 Hex PXI STAR trigger 08 Hex Software triggering 09 Hex Analog level Triggering	Select Trigger source (Combine with select Edge code)
0A Hex	W	00 Hex positive level triggering 10 Hex negative level triggering 20 Hex positive edge triggering 30 Hex negative edge triggering 60 Hex positive edge, continuous triggering 70 Hex negative edge, continuous triggering	Select trigger edge
0A Hex	W	80 Loop counter	Counter loop (0x) or one time (8x)
0B Hex	R and W	(bit0=Do/Di bit1=CLK bit3=CS)	Read Write EEPROM
0C Hex	W	(bit0=DO bit1=CLK bit3=CS)	Write Input offset DAC (16bit)
0D Hex	W	(bit0=DO bit1=CLK bit3=CS) 07 Hex cal offset channel A 08 Hex cal. gain channel A	Write Callibration offset and gain DAC (10bit)
0F Hex	W	00 Hex Lock off 01 Hex ready for trigger	Lock on or off

Channel B

ADDRESS	Operation	DATA	Description
81 Hex	R and W	00000 : 3FFFF Hex	Read or write address counter
82 Hex	R and W	0000 : FFFF (auto increment)	Read or write to memory
84 Hex	W	00 : FF Hex	Write clock source divider (ADC)
85 Hex	R	00 Hex No channel has looped 01 Hex Channel A has looped 02 Hex Channel B has looped 03 Hex Channel A and B looped	Read loop status. Displays if the memory counter has looped one time.
86 Hex	R and W	00 Hex No trigger 01 Hex Trigger channel A 02 Hex Trigger channel B 03 Hex Trigger channel A and B	Write software trigger start. Read current trigger status
87 Hex	W	00 Hex Front clock input 01 Hex Internal clock 70MHz 02 Hex Internal clock 50MHz 10 Hex Front clock out enable	Select Clock source. and Clock output function.
88 Hex	R and W	01 Hex No filter 02 Hex 6MHz filter 04 Hex 15MHz filter 08 Hex 30MHz filter	Select Filter (Combine with Analog output select code)
88 Hex	R and W	10 Hex range 1 input = 1Vpp (x0.2 = 5Vpp) 20 Hex range 2 input = 2Vpp (x0.2 = 10Vpp) 40 Hex range 3 input = 4Vpp (x0.2 = 20Vpp)	Select Attenuator (Combine code with Filter select and input offset)
88 Hex	R and W	80 Hex Input offset on	Input offset on / off (combine with ATT)
89 Hex	R and W	01 Hex Connect input A+ 02 Hex Connect input A- 04 Hex Input A+ 50 Ohm 08 Hex Input A- 50 Ohm 10 Hex Input A+ to GND 20 Hex Input A- to GND 40 Hex input attenuation x 0.2 80 Hex Both inputs AC coupling	Analog output select
8A Hex	W	00 Hex Front trigger 01 Hex PXI trigger 0 02 Hex PXI trigger 1 03 Hex PXI trigger 2 04 Hex PXI trigger 3 05 Hex PXI trigger 4 06 Hex PXI trigger 5 07 Hex PXI STAR trigger 08 Hex Software triggering 09 Hex Analog level Triggering	Select Trigger source (Combine with select Edge code)
8A Hex	W	00 Hex positive level triggering 10 Hex negative level triggering 20 Hex positive edge triggering 30 Hex negative edge triggering 60 Hex positive edge, continuous triggering 70 Hex negative edge, continuous triggering	Select trigger edge
8A Hex	W	80 Loop counter	Counter loop (0x) or one time (8x)
8B Hex	R and W	(bit0=Do/Di bit1=CLK bit3=CS)	Read Write EEPROM
8C Hex	W	(bit0=DO bit1=CLK bit3=CS)	Write Input offset DAC (16bit)
8D Hex	W	(bit0=DO bit1=CLK bit3=CS) 07 Hex cal offset channel A 08 Hex cal. gain channel A	Write Callibration offset and gain DAC (10bit)
8F Hex	W	00 Hex Lock off 01 Hex ready for trigger	Lock on or off

7 Specifications:

PERFORMANCE

ADC Resolution
14 bits each channel

Sample Rate
Internal clock:
500kHz to 70MHz

Absolute Accuracy
±(500μV+ 0.1% of range)
With attenuator on:
±(2.5mV+ 0.2% of range)

Relative Accuracy
±0.025% of range

DC Offset Voltage
-5V to +5V
With attenuator on:
-25V to +25V

Clock Sources
Internal: 70MHz or 50MHz
External: Front panel connector

External Clock Input
Logic Thresholds: V low: < 0.6
V high: > 1.4V
Impedance: 50Ω
Maximum Input: 100MHz

External Clock Output
Clock Levels: V low: < 0.6V
V high: > 1.4V
Impedance: 50Ω

Clock Division Rate
User selectable from 1 to 256
Independent clock source selection per channel

Clock Accuracy
100ppm

Memory Depth
512k-words per channel

Frequency Response
(Referenced at 500kHz)
0 to 20MHz (±0.5dB)
20MHz to 50MHz (±2dB)

TRIGGERING

External Sources

Impedance: 10kΩ DC
Levels: V low: < 0.6V
V high: >2.4V

Internal Sources

PXI STAR
PXI TRIG 0 to 5
Software Trigger, Analog
(Independent trigger source selection per channel)

Polarity

Positive
Negative

Response

Edge
Level

INPUTS

Operating Area

Normal:
-5V to +5V
With attenuator on:
-25V to +25V

Ranges

Normal:
1V (p-p)
2V (p-p)
4V (p-p)
With attenuator on:
5V (p-p)
10V (p-p)
20V (p-p)

Filters

None
30MHz
15MHz
6MHz
(3-pole Butterworth)

SFDR (fs = 50MHz/V in = 2V (p-p)
80dB @ f_{in} = 1MHz
72dB @ f_{in} = 10MHz

SINAD (fs = 50MHz/V in = 2V (p-p))
68dB @ f_{in} = 1MHz
64dB @ f_{in} = 10MHz

Channel Crosstalk
< 70dB @ 1MHz

MAXIMUM CURRENT CONSUMPTION

+3.3V (dc)	300mA
+5V (dc)	650mA
-12V (dc)	40mA
+12V (dc)	40mA

FRONT PANEL INPUTS

Bandwidth (-3dB, filter off)
70MHz

Coupling
DC
AC

Connector
SMB

Impedance (Selectable)
50Ω AC-coupled
50Ω DC-coupled
10KΩ DC-coupled

Input Configuration
Single ended
Differential

ENVIRONMENTAL

Temperature
Operating: 10°C to 50°C
Storage: 0°C to 70°C

Relative Humidity
10% to 80%, non-condensing

Weight
7.4oz (210g)

Module Dimensions
3U high, single width

Product Support

Racal Instruments has a complete Service and Parts Department. If you need technical assistance or should it be necessary to return your product for repair or calibration, call 1-800-722-3262. If parts are required to repair the product at your facility, call 1-949-859-8999 and ask for the Parts Department.

When sending your instrument in for repair, complete the form in the back of this manual.

For worldwide support and the office closes to your facility, refer to the Support Offices section on the following page.

Warranty

Use the original packing material when returning the 2165 to Racal Instruments for calibration or servicing. The original shipping container and associated packaging material will provide the necessary protection for safe reshipment.

If the original packing material is unavailable, contact Racal Instruments Customer Service for information.

Support Offices

RACAL INSTRUMENTS

United States

(Corporate Headquarters and Service Center)
4 Goodyear Street, Irvine, CA 92618
Tel: (800) 722-2528, (949) 859-8999; Fax: (949) 859-7139

5730 Northwest Parkway Suite 700, San Antonio, TX 78249
Tel: (210) 699-6799; Fax: (210) 699-8857

Europe

(European Headquarters and Service Center)
18 Avenue Dutartre, 78150 LeChesnay, France
Tel: +33 (0)1 39 23 22 22; Fax: +33 (0)1 39 23 22 25

29-31 Cobham Road, Wimborne, Dorset BH21 7PF, United Kingdom
Tel: +44 (0) 1202 872800; Fax: +44 (0) 1202 870810

Via Milazzo 25, 20092 Cinisello B, Milan, Italy
Tel: +39 (0)2 6123 901; Fax: +39 (0)2 6129 3606

Racal Instruments Group Limited, Technologie Park,
D-51429 Bergisch Gladbach, Germany
Tel: +49 2204 844205; Fax: +49 2204 844219

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal Instruments Repair Facility.

Model_____ Serial No._____ Date_____

Company Name_____ Purchase Order #_____

Billing Address_____

City

State/Province Zip/Postal Code Country

Shipping Address_____

City

State/Province Zip/Postal Code Country

Technical Contact_____ Phone Number ( )_____
Purchasing Contact_____ Phone Number ( )_____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)

4. Is calibration data required? Yes No (please circle one)
Call before shipping Ship instruments to nearest support office.
Note: We do not accept
“collect” shipments